IN THE CLAIMS

Please enter the following amendments. Amendments have been made to clarify the claims and address informalities.

1. (Previously Amended) A method for generating operationally limited hardware and software, the method comprising:

identifying license information associated with a protected intellectual property block configured for implementation on a device;

generating operationally limited hardware and software, wherein the hardware and software is operationally limited using license information associated with the intellectual property block.

2. (Previously Amended) The method of Claim 1 wherein the license information identifies a parameter associated with a prototype operation range and a production operation range.

3. (Original) The method of Claim 2 wherein the parameter is a hardware parameter.

4. (Original) The method of Claim 3 wherein the hardware parameter is a data format.

5. (Original) The method of Claim 3 wherein the hardware parameter is the number of pin contacts between the hardware and an external device.

6. (Original) The method of Claim 3 wherein the hardware parameter is a signal limit.

7. (Original) The method of Claim 6 wherein the signal limit is a limit on the number of input signals allowed into the hardware by the software.

8. (Original) The method of Claim 6 wherein the signal limit is a limit on the number of output signals allowed out of the hardware by the software.

9. (Original) The method of Claim 8 wherein the output signals are signals used to provide the status of either the hardware or the software.

10. (Original) The method of Claim 3 wherein the parameter is limited by preselected fabrication of the hardware.

11. (Original) The method of Claim 3 wherein the parameter is limited by preselected augmentation of the hardware.

12. (Original) The method of Claim 2 wherein the parameter is a software parameter.

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13. (Original) The method of Claim 12 wherein the parameter is a time limit on run time during which the software will permit operation of the hardware.

14. (Original) The method of Claim 13 further comprising the step of disabling the hardware after the time limit has been attained.

15. (Original) The method of Claim 14 wherein the step of disabling the hardware comprises a reset of a register in the hardware.

16. (Previously Amended) The method of Claim 14 wherein the step of disabling the hardware comprises a global tri-state of the hardware I/O.

17. (Original) The method of Claim 14 wherein disabling the hardware comprises a random failure of the hardware.

18. (Original) The method of Claim 14 wherein an internal clock of the hardware is used to measure the run time of the hardware.

19. (Original) The method of Claim 2 wherein the step of identifying a parameter comprises the step of identifying multiple parameters in accordance with the identification step and further wherein the step of limiting operation of the hardware and software comprises the step of limiting operation of the hardware and software with regard to each identified parameter in accordance with the limitation step.

20. (Previously Amended) The method of Claim 2, wherein the intellectual property block is implemented on a programmable chip.

21. (Previously Amended) The method of claim 20, wherein the programmable chip is a programmable logic device.

22. (Currently Amended) A method for disabling a hardware device, the method comprising:

identifying a run time limit that is (i) long enough to permit testing of the hardware in a prototype manner and (ii) too short for use of the hardware in a production manner, wherein the hardware is a programmable device configured using a software tool having access to a plurality of preconfigured functional blocks;

measuring the time elapsed during operation of the hardware;

disabling the hardware after the time elapsed reaches the run time limit.

23. (Previously Amended) The method of Claim 22 wherein measuring the time elapsed is performed using an internal clock associated with the hardware device.

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24. (Original) The method of Claim 22 wherein disabling the hardware comprises a reset of a register in the hardware.

25. (Previously Amended) The method of Claim 22 wherein disabling the hardware comprises a global tri-state of the hardware I/O.

26. (Original) The method of Claim 22 wherein disabling the hardware comprises a random failure of the hardware.

27. (Previously Amended) The method of Claim 22 wherein disabling is selected from a reset of a register in the hardware, a global tri-state of the I/O of the hardware, and a random failure within the hardware.

28. (Original) A hardware device implementing the method of Claim 22.

29. (Original) The hardware device of Claim 28 wherein the device is a programmable logic device.

30. (Previously Amended) A hardware device, comprising:

a clock;

a memory including a run time limit measured by the clock, the run time limit being (i) long enough to permit testing of the hardware in a prototype manner and (ii) too short for use of the hardware in a production manner, wherein the run time limit is configured at least in part using license information associated with a protected intellectual property block implemented on the hardware device;

circuitry configured to disable the hardware device after the run time limit is reached by the clock.

31. (Previously Amended) The hardware device of Claim 30 wherein the hardware device is disabled using one of the following:

reset of a register in the hardware,

a global tri-state of the I/O of the hardware, and

a random failure within the hardware.

32. (Previously Amended) The hardware device of claim 30, wherein license information is associated with a time limit.

33. (Original) The hardware device of Claim 32, wherein the hardware device is a programmable logic device.

34. (Currently Amended) A computer program product associated with a computer

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readable medium including computer code ~~for~~ which when executed on a computer performs a process of generating operationally limited hardware and software, the computer program product comprising:

computer code for identifying a protected intellectual property block associated with a design;

computer code for identifying a parameter using license information associated with the protected intellectual property block;

computer code for generating operationally limited hardware and software, wherein the hardware and software is operationally limited based on the parameter identified using license information.

35. (Original) The computer program product of Claim 34 wherein the parameter is a hardware parameter.

36. (Original) The computer program product of Claim 35 wherein the hardware parameter is a data format.

37. (Original) The computer program product of Claim 35 wherein the hardware parameter is the number of pin contacts between the hardware and an external device.

38. (Original) The computer program product of Claim 35 wherein the hardware parameter is a signal limit.

39. (Original) The computer program product of Claim 38 wherein the signal limit is a limit on the number of input signals allowed into the hardware by the software.

40. (Original) The computer program product of Claim 38 wherein the signal limit is a limit on the number of output signals allowed out of the hardware by the software.

41. (Original) The computer program product of Claim 40 wherein the output signals are signals used to provide the status of either the hardware or the software.

42. (Original) The computer program product of Claim 35 wherein the parameter is limited by preselected fabrication of the hardware.

43. (Original) The computer program product of Claim 35 wherein the parameter is limited by preselected augmentation of the hardware.

44. (Original) The computer program product of Claim 34 wherein the parameter is a software parameter.

45. (Original) The computer program product of Claim 44 wherein the parameter is a

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time limit on run time during which the software will permit operation of the hardware.

46. (Original) The computer program product of Claim 45 further comprising computer code for disabling the hardware after the time limit has been attained.

47. (Original) The computer program product of Claim 46 wherein disabling the hardware comprises a reset of a register in the hardware.

48. (Original) The computer program product of Claim 46 wherein disabling the hardware comprises a global tri-state of the hardware IO.

49. (Original) The computer program product of Claim 46 wherein disabling the hardware comprises a random failure of the hardware.

50. (Original) The computer program product of Claim 46 wherein an internal clock of the hardware is used to measure the run time of the hardware.

51. (Original) The computer program product of Claim 34 wherein the computer code for identifying a parameter comprises computer code for identifying multiple parameters in accordance with the computer code for identifying the parameter; and further wherein the computer code for limiting operation of the hardware and software comprises computer code for limiting operation of the hardware and software with regard to each identified parameter in accordance with the operation limiting computer code.

52. (Previously Amended) The hardware device of Claim 34, wherein the design is implemented on a programmable chip.

53. (Previously Amended) The hardware device of claim 52, wherein the programmable chip is a programmable logic device.

54. (Currently Amended) A system for generating operationally limited hardware and software, the system comprising:

means for identifying a protected intellectual property block associated with a design;

means for identifying license information associated with the protected intellectual property block;

means for generating operationally limited hardware and software, wherein the hardware and software is operationally limited using license information.

55. (Previously Amended) The system of Claim 54 wherein the license information comprises a first operation range and a second operation range.

56. (Previously Amended) The system of Claim 54 wherein the first operation range and

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the second operation range are mutually exclusive.

57. (Previously Amended) The system of Claim 54 wherein the operational parameter is time and further wherein the first operation range is a prototype testing time range and the second operation range is a production time range.

58. (Previously Amended) The system of Claim 57 wherein the prototype testing time range has a maximum and further wherein the production time range has no maximum.

59. (Previously Amended) The system of Claim 54 wherein the first operation range is a range of timed operation having a maximum time limit and wherein the second operation range is a range of timed operation extending beyond the maximum time limit.

60. (Previously Amended) The system of Claim 59 wherein the second operation range has no maximum time limit.

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